REMARKS

Claims 6, 7 and 14-17 have been cancelled. Claims 1, 8 and 10 have been amended. Claims 18-22 have been added. Claims 1-5, 8-13 and 18-22 are pending. Applicant reserves the right to pursue the original claims and other claims in this and in other applications.

Claims 1-13, 16 and 17 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The rejection is respectfully traversed.

Claim 1 recites a semiconductor integrated circuit device having a "signal transmission part formed in a gate electrode of the semiconductor element [and] a heat conduction part formed in an insulation film on [a] support substrate." Thus, the heat conduction part provides a path different from a signal transmission path provided by the signal transmission part. Applicant respectfully submits that claim 1 and its dependent claims 2-5 and 8-9 are allowable.

Claim 10 contains similar limitations as claim 1 and therefore, claim 10 and its dependent claims 11-13 are likewise allowable.

Claims 1-13, 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Shimada.

The claimed invention relates to a semiconductor integrated circuit device having a semiconductor element formed on a support substrate, the support substrate being a semiconductor substrate or a silicon on insulator (SOI) substrate. In one embodiment, a buried oxide film 3 is formed on a SOI substrate 1 and a plurality of fully-

depletion type MOS transistors are formed on a single crystal silicon layer 5 on the buried oxide film 3. Each of the MOS transistors are electrically separated by oxide films 15 and each MOS transistor has source regions or drain regions 9 and a gate electrode 13. The head conduction part 33, 35, 37, 43, 45 may be connected to the gate electrode 13, to an element separation film 15, or to the source or drain regions 9. The head conduction part may be formed of a plurality of via layers and metal wiring layers. The heat conduction part may be formed such that the heat transmission path is different from a signal transmission path. For more detail, please refer to the drawings, Figures 2-5, and to the specification, pages 17+.

Yamazaki is directed to a semiconductor circuit having a semiconductor element having improved thin film transistor characteristics. The Office Action issued September 21, 2005 cites the "black mask 609" shown by Yamazaki in FIG. 9 as being a heat conduction part. However, the black mask 609 of Yamazaki is produced by forming and patterning a metallic film (column 14, lines 59-62). This manufacturing process results in a black mask 609 made up of a metallic film formed as one solid layer and conforming to the shape of the second interlayer insulating film 607 (Fig. 9, No. 607; column 11, line 25). Therefore, because the black mask 609 is a metallic film formed as one solid layer, it is necessarily made up of only one layer of metal and cannot be construed to "include a plurality of metal wiring layers spaced apart from each other and arranged in a vertical stack" as recited by claim 1. Furthermore, because the black mask 609 is one layer of metal, it does not include "a plurality of metal via layers connected to the metal wiring layers and coupling the metal wiring layers with each other" as is recited by claim 1.

Shimada is directed to wiring boards that have a plurality of wiring layers. The wiring board has a line 1, a shield pattern 2 disposed parallel with line 1 , conductive layers 4, 6, and conductive pillars 7a, 7b that connect the conductive layers 4, 6 (Shimada, FIG. 1). A line 11L and 13L formed on different wiring layers are connected by conductive pillars 7L and shielded by conductive layers 10S, 14S (Shimada, FIG. 3). Neither Yamazaki nor Shimada discloses or teaches a signal transmission part formed in a gate electrode and a heat conduction part formed in an insulation film, i.e., a heat conduction path which is different from a signal transmission path. For at least these reasons, Applicant respectfully submits that claim 1 should be allowable.

Claims 2-5 and 8-13 either depend from claim 1 or contain similar limitations as claim 1. Therefore, claims 2-5 and 8-13 are likewise allowable.

Newly added claims 18-22 are directed to a semiconductor device having inverter cells with a heat conduction part. Neither Shimada nor Yamazaki disclose or teach such a device. For at least these reasons, claims 18-22 should be allowable.

In view of the above, applicant believes the pending application is in condition for allowance.

Dated: December 03, 2007

Respectfully submitted,

By _____
Mark J. Thronson
Registration No.: 33,082
Ranga Sourirajan
Registration No.: 60,109
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicant